M. Tech.

in

VLSI DESIGN

CURRICULUM 2022-23

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA,

SURATHKAL – 575025

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL

Vision

To facilitate transformation of students into good human beings, responsible citizens & competent professionals, focusing on the assimilation, generation and dissemination of knowledge.

Mission

- Impart quality education to meet the needs of profession and society, and achieve excellence in teaching-learning and research.
- Attract and develop talented and committed human resources, and provide an environment conducive to innovation, creativity, team-spirit and entrepreneurial leadership.
- Facilitate effective interactions among faculty and students, and foster networking with alumni, industries, institutions and other stake-holders.
- Practice and promote high standards of professional ethics, transparency and accountability.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Vision

To be a model for academic excellence in the area of Electronics & Communication Engineering.

Mission

M1. Impart quality teaching-learning-experience with state-of-the-art curriculum.

M2. Enhance Research, Consultancy and Outreach activities.

M3. Increase the visibility of academic programs globally and attract talent at all levels.

M4. Foster sustained interaction with the alumni, industries, R & D organizations, world class universities and other stakeholders to stay relevant in the globalized environment.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

M. Tech. in VLSI Design (VL)

Program Educational Objectives (PEOs)

PEO1: Practice Electronics and Communication engineering in a successful professional career.

PEO2: Pursue higher education and / or research for professional development.

PEO3: Contribute as an individual or a team member with demonstrable attributes in lifelong learning for the welfare of the society.

Program Outcomes (POs)

PO1: An ability to independently carry out research/investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: An ability to demonstrate a degree of mastery in VLSI Design.

PO4: An ability to apply appropriate techniques and modern engineering tools in the design and implementation in the area of VLSI Design

PO5: An ability to apply engineering and management principles in multi-disciplinary environment through their team playing and self-learning capabilities.

M. Tech. in VLSI Design (VL)

Suggested Plan of Study:

Sl. No.	Semester			
	I	II	III	IV
1	EC701	EC703	EC729	EC730
2	EC702	EC704		
3	EC791	EC792		
4	EC705	Elective 3		
5	Elective 1	EC727		
6	Elective 2	EC728		

Credit Requirements:

Category	Minimum Credits to be Earned
Program Core (Pc)	26
Elective Courses (Ele.)	12
Mandatory Learning Courses (MLC)	04
Major Project (MP)	12
Total	**54**

Program Core (PC)

EC701	CMOS VLSI	(4-0-0) 4
EC702	Analog Integrated Circuit Design	(4-0-0) 4
EC703	VLSI Data Converters	(4-0-0) 4
EC704	VLSI Design Automation	(4-0-0) 4
EC705	IC Design Lab	(0-0-3) 2
EC791	Linear Algebra and Stochastic Processes	(4-0-0) 4
EC792	High Performance Computing Architectures	(4-0-0) 4

Electives (E)

(At least ONE elective must be chosen from this list)

EC801	Logic Synthesis Techniques	(4-0-0) 4
EC802	Low Power VLSI Design	(4-0-0) 4
EC803	Microelectronic Devices	(4-0-0) 4
EC804	Digital VLSI Testing & Testability	(4-0-0) 4
EC805	Embedded Systems	(2-0-3) 4
EC806	Digital Design using FPGAs	(2-0-3) 4
EC807	Active Filter Design	(4-0-0) 4
EC808	CMOS RF Integrated Circuits	(4-0-0) 4
EC809	Heterogeneous and Parallel Programming	(2-0-3) 4
EC870	Architectures for Signal Processing and Machine Learning	(4-0-0) 4

Mandatory Learning Courses (MLC)

EC727	Seminar	2
EC728	Minor Project	2

Major Project (MP)

EC729	Major Project - I	4
EC730	Major Project - II	8

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
M.Tech. in VLSI Design

CORE COURSES

EC701 CMOS VLSI (4-0-0) 4

Course Outcomes:
CO1: Understand the device MOSFET and design MOSFET based logic circuits and logic gates
CO2: Analyse the MOSFET based logic circuits with parasitic elements associated with them and optimize the circuit performance
CO3: Design and analyze basic VLSI sub-systems
CO4: Evaluate the MOSFET based logic circuits using circuit simulation software

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	3	1
CO2	3	1	3	3	2
CO3	3	1	3	3	2
CO4	3	2	3	3	3

Course Contents
MOSFET - Review of current equation, regions of operation, MOSFET logic circuits. MOSFET logic gates. Interfacing CMOS and Bipolar logic families. Circuit characterization and performance estimation, Switching characteristics, Delay models, Power dissipation, Packaging, Scaling of MOS transistor dimensions, Yield and Reliability, CMOS subsystem design, Datapath operations, Addition, Multiplication, Counters, Shifters, Memory design. Interconnect design, Power-grid and clock design. Simulation exercises on MOSFET.

References
Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic Digital Integrated Circuits – A design perspective, Pearson, 2003
S. M. Kang & Y. Leblebici, CMOS Digital Integrated Circuits, McGraw Hill, 1999.
David A Hodges, Horace G. Jackson and Resve Saleh, Analysis and Design of Digital Integrated Circuits, Mc GrawHill, 2003
Neil H. E. Weste, David Money Harris, Integrated Circuit Design, Fourth Edition, 2011
NPTEL Video Lectures

EC702 ANALOG INTEGRATED CIRCUIT DESIGN (4-0-0) 4

Course Outcomes:
CO1: Understand the importance of the MOSFET as a component in analog VLSI circuits.
CO2: Analyze MOSFET based circuits for DC operating point and small-signal behaviour.
CO3: Design single ended and differential amplifiers.
CO4: Design two stage fully differential amplifier and evaluate its performance for closed loop applications.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	2	1
CO2	3	1	3	2	1
CO3	3	1	3	2	1
CO4	3	2	3	2	2

Course Contents
MOSFET - Review of current equation, regions of operation, small signal model. Current mirrors, Single-ended amplifiers, Differential amplifiers, Two-stage amplifiers – analysis, frequency response, stability, compensation; Band gap references, Constant–Gm biasing; Types of Noise, Introduction to switched capacitor circuits, switched capacitor amplifiers, noise analysis, Distortion, current and voltage references, Oscillators and PLL.

References

Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill International Edition 2016
Behzad Razavi, Fundamentals of Microelectronics, Second edition, Wiley, 2013
Sedra and Smith, Microelectronics Circuits, Oxford Univ. Press, 2004
David A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley, 2002
Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2003.
NPTEL Video Lectures

EC703 VLSI DATA CONVERTERS (4-0-0) 4

Course Outcomes:

CO1: Develop basic understanding of CMOS circuit realization of ADCs and DACs.
CO2: Apply the concepts and analyze various architectures of ADCs and DACs.
CO3: Analyze and quantify the effects of non-idealities on the performance of ADCs and DACs.
CO4: Design basic ADCs and DACs.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	1	-	1
CO2	3	1	2	-	1
CO3	3	1	3	1	1
CO4	3	1	3	1	1

Course Contents

Sample and Hold Circuits: Basic S/H circuit, effect of charge injection, compensating for charge injection, bias dependency, bias independent S/H. D/A Converter – General considerations, Static non-idealities and Dynamic nonidealities; Current-steering DAC – Binary weighted DAC, Thermometer DAC, Design issues, Effect of Mismatches. A/D converter – General considerations, static and dynamic non-idealities. Flash ADC – Basic architecture, Design issues, Comparator and Latch, Effect of non-idealities, Interpolative and Folding architectures. Successive Approximation ADC; Pipeline ADC. Over sampling ADC – Noise shaping, Sigma-Delta modulator.

References

Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill International Edition 2016
David A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley, 2002
Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2003.
Behzad Razavi, Principles of Data Conversion System Design, Wiley-IEEE Press, 1995
Rudy J. van de Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, Springer, 2003
NPTEL Video Lectures

EC704 VLSI DESIGN AUTOMATION (4-0-0) 4

Course Outcomes:

CO1: Understand and analyze various phases of physical design automation of a digital VLSI system.
CO2: Transform the structural representation of a digital VLSI system into a graph.
CO3: Apply various physical design algorithms for partitioning, floor planning, placement and routing of a digital system and analyze their trade-offs.
CO4: Develop a prototype EDA tool to transform a circuit level netlist into an optimized layout.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	2	2	2
CO2	3	1	2	-	2
CO3	3	1	2	3	2
CO4	3	2	2	3	3

Course Contents

Introduction to VLSI design automation: VLSI design methodologies, use of VLSI EDA tools, Algorithmic Graph Theory, computational Complexity; Partitioning, Simulated Annealing. Floor planning and placement, Routing, High Level Synthesis, operation scheduling, Static Timing Analysis, Topological vs logical timing analysis, False paths, Arrival time, Required arrival Time, Slacks. Advanced VLSI Design Automation: Physical Synthesis, Optical Proximity correction, Interconnect issues.

References

Kahng AB, Lienig J, Markov IL, Hu J. VLSI physical design: from graph partitioning to timing closure, Springer; 2011.
Wang LT, Chang YW, Cheng KT, editors. Electronic design automation: synthesis, verification, and test, Morgan Kaufmann; 2009.
Alpert CJ, Mehta DP, Sapatnekar SS, editors. Handbook of algorithms for physical design automation, CRC press; 2008.
Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer, 2008
Naveed Sherwani, Algorithms for VLSI Physical Design Automation, 3rd ed., Kluwer Academic Pub., 1999
Majid Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996.
Sabih H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998
Sadiq M. Sait & Habib Youssef, VLSI Physical Design Automation: Theory and Practice, World Scientific Publishing, 1999
NPTEL Video Lectures

EC705 IC DESIGN LAB (0-0-3) 2

Course Outcomes:

CO1: Design MOSFET based logic circuits, logic gates and analog circuit blocks using circuit simulation softwares
CO2: Analyse the effects of non-idealities of devices on the circuit performance and mitigate the effects.
CO3: Create layout of logic circuits using EDA tools, analyze the extracted netlist and optimize the performance through post-layout simulations
CO4: Design basic VLSI subsystems for given specifications.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	3	3	3	1
CO2	3	3	3	3	2
CO3	3	3	3	3	2
CO4	3	3	3	3	3

Course Contents

Design, Simulation and layout of basic digital blocks, performance comparison, Design project Tools to be used: CADENCE, MAGIC, SPICE, ELECTRIC, Mentor Graphics

EC791 LINEAR ALGEBRA AND STOCHASTIC PROCESSES (3-1-0) 4

Course Outcomes:

CO1: Understand and solve elementary problems involving concepts of vector spaces, matrices, probability theory and random variables.
CO2: Apply, analyse and solve problems based on advanced concepts on matrix decomposition and stochastic processes.
CO3: Derive mathematical models to describe the working of communication systems, crypto systems, image and speech processing systems and certain VLSI systems/ devices.
CO4: Design Monte Carlo simulation platforms to simulate the functioning of a few selected modern signal processing/ communication/ VLSI systems.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	2	1	2	1	1
CO2	2	2	2	2	1
CO3	2	2	1	3	2
CO4	2	2	2	3	2

Course Contents

Vector Spaces, Subspaces, Linear Independence, Span, Basis, Dimension, Linear Transformations, Orthogonal Transformations, Orthogonal projections, Matrix subspaces and orientation, Eigen decomposition, SVD, Least Squares, Pseudo inverse.

Review of Probability theory and Random variables, Random vectors and moments, Stochastic Processes and Examples, stochastic processes and linear systems, Gaussian random process, spectral analysis of stationary processes, Power Spectral Densities, Stationarity and Ergodicity.

References

Gilbert Stran, Linear algebra and its applications, Thomson Brooks, 2006.
P Halmos, Finite Dimensional Vector Spaces, Springer, 1993.
Edgar G. Goodaire, Linear Algebra: Pure & Applied, World Scientific, 2014.
Dimitris P. Bertsekas, John N. Tsitsiklis, Introduction to Probability, 2nd Ed, Athena Scientific, 2008.
Alberto Leon-Garcia, Probability, Statistics, and Random Processes for Electrical Engineering, 3rd Ed, Addison-Wesley, 2008.

EC792 HIGH PERFORMANCE COMPUTING ARCHITECTURES (4-0-0) 4

Course Outcomes:

CO1: Understand basic aspects of high-performance computer architectures
CO2: Perform quantitative analysis of modern computing systems
CO3: Evaluate the performance of available choices for exploiting parallelism in Instruction, data and memory
CO4: Design a representative high performance computing subsystem/system within the given constraints

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	-	-
CO2	3	1	3	1	1
CO3	3	1	3	2	2
CO4	3	3	3	3	2

Course Contents

Instruction Level Parallelism: Pipelining, Hazards, Instruction Level Parallelism, Branch prediction, Static and Dynamic Scheduling, Speculation, Limits of ILP. Multicore Memory Hierarchy: Cache trade-offs, Basic and Advanced optimizations, Virtual Memory, DRAM optimizations. Multiprocessors: Symmetric and Distributed architectures, Cache coherence protocols - Snoopy and Directory based, ISA support for Synchronization, Memory Consistency Models. Interconnection Networks: Architectures, Topologies, Performance, Routing, Flow control, Future of NoCs.

References

J. Hennessy and D. Patterson, Computer Architecture–A Quantitative approach, Morgan Kaufmann, 6th Ed., 2017.
David A. Patterson and John L. Hennessy, Computer Organization and Design RISC-V Edition: The Hardware Software Interface, Morgan Kaufman, 2017.
Recent processor architectures from Intel / TI
John Paul Shen and Mikko H. Lipasti, Modern Processor Design: Fundamentals of Superscalar Processors, Tata McGraw Hill, 2013
Behrooz Parhami, Computer Arithmetic Algorithms and Hardware Design, Oxford, 2000.
MOOC Courses

ELECTIVE COURSES

EC801 LOGIC SYNTHESIS TECHNIQUES (4-0-0) 4

Course Outcomes:

CO1: Use BDD as a tool for binary logic representation and minimization
CO2: Apply and analyze heuristic minimization algorithms to optimize 2-level and multi-level logic circuits
CO3: Analyze algorithms to do retiming, static timing analysis and extract timing data in logic circuits
CO4: Create an optimized logic function from an arbitrary complex logic function

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	2	2	1
CO2	3	1	3	2	1
CO3	3	1	3	2	1
CO4	3	3	3	3	2

Course Contents

Introduction to Computer aided synthesis and optimization. Hardware Modeling. Advanced Boolean Algebra and Applications, Shannon co-factors, satisfiability and cover, Binary Decision Diagrams, Representing Boolean functions, ROBDD, ITE operator, Variable ordering- choice of variables, application of BDD to synthesize Boolean functions, Two-level combinational logic optimization, Multi-level combinational optimization. Sequential logic optimization. Cell Library Binding. Algorithms for Technology mapping – Structural and Boolean matching, Simulation & Static Timing analysis - Event driven simulation – zero delay, unit delay and nominal delay simulation, Timing analysis at the logic level, Delay models, Delay graph, static sensitization, State of the art and future trends: System level synthesis and hardware software co-design.

References

Giovanni De Micheli, Synthesis and Optimization of Digital Circuits, McGraw Hill, 1994.
Sunil P. Khatri · Kanupriya Gulati, Editors, "Advanced Techniques in Logic Synthesis, Optimizations and Applications", Springer publications, 2011.
S. Hassoun and T. Sasao, (Editors), Logic Synthesis and Verification, Kluwer Academic publishers, 2002
Srinivas Devadas, Abhijith Ghosh and Kurt Keutzer, Logic Synthesis", Kluwer Academic, 1998.
G. D. Hachtel and F. Somenzi, Logic Synthesis and Verification Algorithms, Kluwer Academic Publishers, 1996.
NPTEL Video Lectures

EC802 LOW POWER VLSI DESIGN (4-0-0) 4

Course Outcomes:

CO1: Understand various sources of power consumption in VLSI circuits and systems.
CO2: Understand and analyse various power estimation techniques.
CO3: Analyze various power reduction strategies at different levels of design abstractions.
CO4: Evaluate design strategies of low power VLSI circuits.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	-	1
CO2	3	1	3	-	1
CO3	3	1	3	1	2
CO4	3	1	3	1	2

Course Contents

Introduction to Low Power VLSI. Modeling and Sources of Power consumption. Power estimation at different design levels. Power optimization for combinational circuits and sequential circuits Voltage scaling Approaches. Low energy computing using energy recovery techniques. Low Power SRAM architectures. Software design for low power. Computer Aided Design Tools. Case studies Recent trends in low-power design for mobile and embedded application.

References

Kaushik Roy, Sharat Prasad, Low-Power CMOS VLSI design, John Wiley, 2000.
K.-S. Yeo and K. Roy, Low-Voltage Low-Power Subsystems, McGraw Hill, 2004.
L. Benini and G. De Micheli, Dynamic Power Management Design Techniques and CAD Tools, Springer, 1998.
S. G. Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies, Springer, 2005.
Edgar Sánchez-Sinencio, Andreas G. Andreou, Low-Voltage/Low-Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits IEEE Press Series on Microelectronic Systems 1999
NPTEL Video Lectures

EC803 MICROELECTRONIC DEVICES (4-0-0) 4

Course Outcomes:
CO1: Understand the advanced physical concepts in semiconductor materials
CO2: Apply concepts of semiconductor materials to develop understanding of commonly used semiconductor devices.
CO3: Analyze the effect of technology scaling on semiconductor devices.
CO4: Evaluate the device performance improvement for various device engineering techniques.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	-	-
CO2	3	1	3	-	-
CO3	3	1	3	2	2
CO4	3	1	3	3	2

Course Contents
Review of basic device physics, Electronic structure of semiconductors, Diodes, MOS capacitor. Transistor theory. Scaling - Moore's law on technology scaling, MOS device scaling theory, Short channel effects, sub threshold leakage, Punch through, DIBL, High field mobility, Velocity saturation and overshoot. Reliability. Various definitions of channel length, Performance metric of digital technology, Transistor design trade-offs, Technology case studies, Silicon on Insulator (SOI) devices, Partially depleted and fully depleted SOI, Floating body effects, SOI for low power, Interconnects in sub-micron technology, Foundry technology, International Technology Roadmap for Semiconductors (ITRS)

References
J. A. del Alamo Integrated Microelectronic Devices: Physics and Modeling, Pearson, 2017
Yaun Taur, Tak H. Ning, Fundamentals of modern VLSI devices, Cambridge university press, 1998.
B. G. Streetman & S. Banerjee, Solid State Electronic Devices, Prentice Hall, 1999.
M. K. Achuthan and K. N. Bhat, Fundamentals of Semiconductor Devices, McGraw Hill, 2006
Nandita Dasgupta, Amitava Dasgupta, Semiconductor Devices: Modelling And Technology, Phi, 2009
A. K. Dutta, Semiconductor Devices and Circuits, Oxford Univ. Press, 2008.
ITRS Road map - http://public.itrs.net/
NPTEL Video Lectures

EC804 DIGITAL VLSI TESTING & TESTABILITY (4-0-0) 4

Course Outcomes:
CO1: Understand the role of test generation and test application in VLSI design flow
CO2: Analyze different fault models and test generation techniques
CO3: Demonstrate fault list and test pattern generation for a given gate-level netlist.
CO4: Design logic subsystem conforming to testability requirements

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	1	-
CO2	3	1	3	2	1
CO3	3	2	3	3	1
CO4	3	2	3	2	2

Course Contents
Overview of testing and verification, Defects and their modeling as faults at gate level and transistor level. Functional V/s. Structural approach to testing. Complexity of testing problem. Controllability and observability. Generating test for a signal stuck-at-fault in combinational logic. Algebraic algorithms. Test optimization and fault coverage. Logic Level Simulation – Delay Models, Event driven simulation, general fault simulation (serial, parallel, deductive and concurrent). Testing of sequential circuits. Observability through the addition of DFT hardware, Adhoc and structured approaches to DFT – various kinds of scan design. Fault models for PLAs, bridging and delay faults and their tests. Memory testing, testing with random patterns. LFSRs and their use in random test generation and response compression (including MISRs), Built-in self-test.

References

M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1994.
M. L. Bushnel and V. D. Agarwal, Essentials of Testing for Digital, Memory and Mixed – Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
Ajai Jain, Learning Module for the course - VLSI Testing and Testability, IIT, Kanpur, 2001.
NPTEL Video Lectures

EC805 EMBEDDED SYSTEMS (2-0-3) 4

Course Outcomes:

CO1: Understand the differences between the general computing system and the embedded system, also recognize the classification of embedded systems.
CO2: Analyze various components of embedded hardware and software.
CO3: Design a medium complexity embedded system under specified design constraints.
CO4: Analyze various examples of embedded systems based on their design and evaluate their performance critical points.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	-	2	1	1
CO2	3	-	3	1	1
CO3	2	1	3	2	3
CO4	3	1	3	3	3

Course Contents

Introduction: Overview of embedded systems, embedded system design challenges, common design metrics and optimizing. Survey of different embedded system design technologies & trade-offs. Embedded microcontroller cores, embedded memories, Examples of embedded systems. Architecture for embedded system, High performance processors – strong ARM processors, programming, interrupt structure, I/O architecture, Technological aspects of embedded systems: interfacing between analog and digital blocks, signal conditioning, Digital signal processing, Subsystem interfacing, interfacing with external systems. Software aspects of embedded systems: real time programming languages and operating systems for embedded systems – RTOS requirements, kernel types, scheduling, context switching, latency, inter-task communication and synchronization, Case studies.

References

Jack Ganssle, The Art of Designing Embedded Systems, Elsevier, 1999.
R. Gupta, Co-synthesis of Hardware and Software for Embedded Systems, Kluwer 1995.
Steve Furber, "ARM System Architecture", Edison Wesley Longman, 1996.
Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", Elsevier, 2004.
NPTEL Video Lectures

EC806 DIGITAL DESIGN USING FPGAs (2-0-3) 4

Course Outcomes:

CO1: Design simple digital systems given a set of specifications
CO2: Model digital systems using HDL given a set of specifications
CO3: Appreciate architecture of FPGAs and implement digital sub-systems using FPGAs
CO4: Design and Implement digital system using FPGAs for target application

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	1	1
CO2	3	2	3	3	1
CO3	3	2	3	3	1
CO4	3	3	3	3	3

Course Contents

Digital system design options and trade-offs, Design methodology and technology overview, High Level System. Architecture and Specification: Behavioral modeling and simulation, Overview of FPGA architectures and technologies, Logic block architecture, Input and Output cell characteristics, clock input, Timing, Power dissipation, Programmable interconnect, Applications, Embedded system design using FPGAs, Dynamic architecture using FPGAs, reconfigurable systems, application case studies, Simulation / implementation exercises of combinational, sequential and DSP kernels on Xilinx / Altera boards.

References

M.J.S. Smith, Application Specific Integrated Circuits, Pearson, 2000
Peter Ashenden, Digital Design using VHDL, Elsevier, 2007
Peter Ashenden, Digital Design using Verilog, Elsevier, 2007
Clive Maxfield, The Design Warriors's Guide to FPGAs, Elsevier, 2004
NPTEL Video Lectures

EC807 ACTIVE FILTER DESIGN (4-0-0) 4

Course Outcomes:

CO1: Derive the transfer function of the filter for Butterworth and Chebyshev filter responses.
CO2: Synthesize the passive filter network for the given transfer function.
CO3: Transform a given passive filter network into Gm-C and Active-RC filter.
CO4: Design and implement a CMOS active filter and evaluate its performance.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	2	3	1
CO2	3	1	2	3	1
CO3	3	1	2	3	1
CO4	3	2	2	3	3

Course Contents

Butterworth, Chebyshev & Inverse-Chebyshev filter response and pole locations; LC ladder filter – prototype & synthesis; Frequency transformation of lowpass filter. Impedance converters; Gm-C filters – Gm-C biquad, Q enhancement, Automatic Tuning; Active-RC filters – Comparison with Gm-C filter, Issues in realizing high frequency active-RC filters; Characterization of on-chip integrated continuous time filters.

References

R. Schaumann and M.E. Van Valkenburg, Design of Analog Filters, Oxford University Press, 2003.
P. V. Ananda Mohan, Current-Mode VLSI Analog Filters - Design and Applications, Birkhauser, 2003
NPTEL Video Lectures

EC808 CMOS RF INTEGRATED CIRCUITS (4-0-0) 4

Course Outcomes:

CO1 Understand RF Design issues and required circuit theory
CO2 Understand, design and analyse RF Transceiver Architectures
CO3 Design and analyze matching networks using RF/microwave CAD software for RF applications
CO4 Design and analyze RF functional blocks and circuits

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	2	-	2	1	1
CO2	3	1	3	2	2
CO3	3	1	3	3	2
CO4	3	2	3	3	2

Course Contents

Basic concepts in RF Design – harmonics, gain compression, desensitization, blocking, cross modulation, intermodulation, inter symbol interference, noise figure, Friis formula, sensitivity and dynamic range; Receiver

architectures – heterodyne receivers, homodyne receivers, image-reject receivers, digital-IF receivers and subsampling receivers; Transmitter architectures – direct-conversion transmitters, two-step transmitters; Low noise amplifier (LNA) – general considerations, input matching, CMOS LNAs; Down conversion mixers – general considerations, spur-chart, CMOS mixers; Oscillators – Basic topologies, VCO, phase noise, CMOS LC oscillators; PLLs – Basic concepts, phase noise in PLLs, different architectures.

References

Behzad Razavi, RF Microelectronics, Prentice Hall PTR, 1997
Thomas H. Lee, The design of CMOS radio-frequency integrated circuit, Cambridge University Press, 2006
Chris Bowick, RF Circuit Design, Newnes, 2007
NPTEL Video Lectures

EC809 HETEROGENEOUS AND PARALLEL PROGRAMMING (3-0-2) 4

Course Outcomes:

CO1: Understand the Heterogeneous Computing Platforms and the GPU architecture.
CO2: Understand the OpenCL device architecture, concurrency and execution models.
CO3: Develop and analyse OpenCL Code for simple designs.
CO4: Apply the parallel programming concepts to computationally intensive applications like speech analysis, image convolution etc.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	2	1	3	2	1
CO2	2	1	1	2	1
CO3	2	2	2	3	1
CO4	2	2	2	3	2

Course Contents

Heterogeneous platform and GPU architecture. Introduction to OpenCL. OpenCL device architecture. Concurrency and execution model. Programming examples like vector addition, convolution and matrix multiplication. Application case studies.

References

Benedict R. Gaster, Lee Howes, David R. Kaeli, Perhaad Mistry, Dana Schaa, "Heterogeneous Computing with OpenCL" - Revised OpenCL 1.2 Edition, Morgan Kaufmann, 2013.
Aaftab Munshi, Benedict R. Gaster, Timothy G. Mattson, James Fung, Dan Ginsburg, "OpenCL Programming Guide", Addison-Wesley, 2012.
David B. Kirk and Wen-mei W. Hwu, "Programming Massively Parallel Processors - A Hands-on Approach", Second Edition, Morgan Kaufmann, 2013.
NPTEL Video Lectures

EC870 ARCHITECTURES FOR SIGNAL PROCESSING AND MACHINE LEARNING (4-0-0) 4

Course Outcomes:

CO1: Understand basic aspects of digital signal processing systems and architectures.
CO2: Use Data Flow Graphs (DFG) to represent computational blocks in a DSP system.
CO3: Apply and analyse algorithms of retiming, folding, unfolding etc. used for optimizing DSP system architectures.
CO4: Design and analyse DSP architecture modules for complex operations such as fast convolution, matrix multiplication, filtering, etc.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	2	2	2
CO2	3	1	2	2	2
CO3	3	1	3	2	2
CO4	3	1	3	3	2

Course Contents

Representation of digital signal processing systems: block diagrams, signal flow graphs, data-flow graphs, dependence graphs; pipelining and parallel processing for high-speed and low power realizations; iteration bound, algorithms to compute iteration bound, retiming of data-flow graphs; unfolding transformation of data-flow graphs; systolic architecture design, architectures for real and complex fast Fourier transforms; stochastic logic based computing, computing digital filters, arithmetic functions and machine learning functions using stochastic computing; Neural Network architectures.

References

K.K. Parhi, VLSI Digital signal processing systems: Design and implementation, John Wiley, 1999.
Lars Wanhammar, DSP Integrated Circuits, Academic Press, 1999.
Sen M. Kuo Bob H. LeeWenshun Tian, Real-Time Digital Signal Processing: Implementations and Applications, John Wiley & Sons, Ltd, 2006.
Roger Woods, John McAllister, Gaye Lightbody, Ying Yi, FPGA Based Implementation of Signal Processing Systems, John Wile, 2017.
U. Meyer-Baese, Digital Signal Processing with Field Programmable Gate Arrays, 4th Ed. Springer, 2014.
Recent literature.

EC727 Seminar 2

Course Outcomes:

CO1: Understanding various resource materials on a particular topic.
CO2: Apply and collate the knowledge on the chosen topic.
CO3: Analyse and evaluate the topic and bring it to a presentable form.
CO4: Effectively communicate the technical information through a report and oral presentation demonstrating expertise earned on the chosen topic.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	2	-	1
CO2	3	1	2	-	2
CO3	3	1	3	3	2
CO4	3	3	3	3	2

Course Contents

Seminar topics on the recent advancements in VLSI Design and related areas.

EC728 Minor Project 2

Course Outcomes:

CO1: Conduct literature survey and identify a reasonable problem in VLSI domain.
CO2: Apply the technical knowledge gained in the domain and devise a strategy to address the problem formulated.
CO3: Analyse and execute the project using relevant tools.
CO4: Communicate technical project information by preparing research reports and oral presentations demonstrating the expertise gained.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	1	2
CO2	3	1	3	1	3
CO3	3	2	3	3	3
CO4	3	3	3	3	3

EC729 Major Project – I 4

Course Outcomes:

CO1: Identify engineering problems relevant to the domain of VLSI Design and suggest possible solutions.
CO2: Apply the technical knowledge gained in the domain to execute the project work.
CO3: Learn project management skills and implement the proposed project using relevant tools.
CO4: Evaluate the solution and communicate technical project information through research reports and oral presentations demonstrating mastery in the chosen problem

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	1	2
CO2	3	1	3	3	3
CO3	3	2	3	3	3
CO4	3	3	3	3	3

EC730 Major Project – II 8

Course Outcomes:

CO1: Identify engineering problems relevant to the domain of VLSI Design and suggest possible solutions.
CO2: Apply the technical knowledge gained in the domain to execute the project work.
CO3: Learn project management skills and implement the proposed project using relevant tools.
CO4: Evaluate the solution and communicate technical project information through research reports and oral presentations demonstrating mastery in the chosen problem

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5
CO1	3	1	3	1	2
CO2	3	1	3	3	3
CO3	3	2	3	3	3
CO4	3	3	3	3	3

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